

# WM3G6-15 Digital Systems Design

**26/27**

**Department**

WMG

**Level**

Undergraduate Level 3

**Module leader**

Siavash Amin-Nejad

**Credit value**

15

**Module duration**

14 weeks

**Assessment**

60% coursework, 40% exam

**Study locations**

University of Warwick main campus, Coventry Primary

Distance or Online Delivery

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## Description

### Introductory description

Digital systems design using hardware description languages (Verilog, VHDL, ...) and implementation on CPLDs and FPGAs is now an standard design and development method. This module initially covers fundamentals of digital electronics which is necessary for the next part of the module which introduces students to the Verilog HDL. Simulation and synthesis tools from a leading FPGA manufacture for design, test and implementation on FPGA boards will be practised by students as the concluding part of this module.

This modules is linked with C1, C3, C12, C13, C17 of AHEP 4.

LO1: C1, C3

LO2: C1, C3

LO3: C1, C3

LO4: C12, C13, C17

[Module web page](#)

### Module aims

The first aim of this module is to introduce students to the fundamentals of combinatorial and sequential logic circuit design. The second aim which is built on the first one is to enable students

to use hardware description languages and verification tools to design digital systems.

## Outline syllabus

This is an indicative module outline only to give an indication of the sort of topics that may be covered. Actual sessions held may differ.

- Combinational logic circuit design ( truth table, Karnaugh map, logic gates)
- Logic Functions - Multiplexer, Demultiplexer, Decoder, Adder
- Sequential logic circuit design ( flip-flops, shift registers and counters)
- Finite State Machines - synchronous design
- Mealy and Moore state machines
- Metastability - Setup and Hold times
- Hardware description languages. Verilog modelling concepts. Concurrent and sequential statements.
- Structural, data flow and behavioural architecture descriptions
- Design methodology. Top down design. Register-transfer-level design. Test benches.
- Simulation and Synthesis of Verilog designs on a FPGA development board.
- Introduction to Programmable Logic Devices (FPGAs, CPLDs)

## Learning outcomes

By the end of the module, students should be able to:

- Design basic combinatorial logic circuits like adders and multiplexers [AHEP:4- C1, C3]
- Create Mealy and Moore finite state machines for sequential circuits [AHEP:4- C1, C3]
- Produce Verilog descriptions of digital data-path components and finite state machines [AHEP:4- C1,C3]
- Design and implement simple synchronous digital systems using FPGA hardware [AHEP: 4- C12, C13, C17]

## Indicative reading list

[Reading lists can be found in Talis](#)

## Subject specific skills

- Interpret and produce technical documentation such as schematic and circuit diagrams, engineering drawings or CAE models, simulation models, project plans, engineering reports, test reports, fault reports or data analytics using company documentation systems and guidelines. ( S4 in ST0024)
- Observe, record and draw accurate and auditable conclusions from data and/or developmental or test evidence. (S5 in ST0024)
- Ensure that all systems or testing/prototyping equipment has been correctly configured and checked for safe operation before use. (S13 in ST0024)

## Transferable skills

- Digital literacy
  - Information literacy
  - Critical thinking.
  - Problem-solving.
  - Teamwork
  - Communication
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## Study

### Study time

Type	Required
Lectures	6 sessions of 1 hour (4%)
Seminars	6 sessions of 1 hour (4%)
Practical classes	6 sessions of 1 hour (4%)
Online learning (scheduled sessions)	12 sessions of 1 hour (8%)
Online learning (independent)	5 sessions of 1 hour (3%)
Other activity	5 hours (3%)
Private study	50 hours (33%)
Assessment	60 hours (40%)
Total	150 hours

### Private study description

Self-guided study: revision on module contents, solution of additional seminar-type questions, video tutorials and supplementary materials.

Study and advanced use of simulation software.

Analyzing datasheets of components.

Online forum forum for discussing queries with course peers and tutors. (asynchronous).

### Other activity description

- Preparation for the practical lab.
- Online consulting session for providing one to one support to help struggling students.

## Costs

No further costs have been identified for this module.

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# Assessment

You must pass all assessment components to pass the module.

## Assessment group D

Assessment component	Weighting	Study time	Eligible for self-certification
Design and implementation of digital systems on FPGA Individual written assignment: Analysis and discussion of simulations and experiments. Experiments will be done in Groups of 3 (possibly 2), but the report is written and submitted individually. (LO3 and LO4)	60%	36 hours	Yes (extension)

### Reassessment component

Design and implementation of digital systems on FPGA Individual written assignment: Analysis and discussion of simulations and experiments. Experiments will be done in Groups of 3 (possibly 2), but the report is written and submitted individually. (LO3 and LO4)			No
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### Assessment component

Exam Exam for testing students' knowledge of designing combinatorial and sequential logic circuits.	40%	24 hours	No
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Reassessment component is the same

## Feedback on assessment

Formative Feedback:

- Verbal individual feedback given during seminar/tutorial sessions.

Summative feedback:

- Written cohort level feedback on the exam.
- Written individual feedback on the written report.

## Availability

## Courses

This module is Core for:

- Year 3 of UWMS-H7C2 Undergraduate Applied Professional Engineering (Electrical/Electronic Support Engineer)
- Year 3 of DWMS-H7C6 Undergraduate Applied Professional Engineering (Electrical/Electronic Support Engineer) (Degree Apprenticeship)