ES2E3-15 Digital Systems Design

23/24

Department
School of Engineering
Level
Undergraduate Level 2
Module leader
Eduardo Wachter
Credit value
15
Module duration
10 weeks
Assessment
50% coursework, 50% exam
Study location
University of Warwick main campus, Coventry

Description

Introductory description

n/a.

Module web page

Module aims

To introduce students to the principles and practice of designing digital electronic circuits, with a focus on field programmable gate array implementation, including the tool flow, architecture, testing, and design for performance.

Outline syllabus

This is an indicative module outline only to give an indication of the sort of topics that may be covered. Actual sessions held may differ.

Recap of combinational and sequential circuits: gates, multiplexers, encoders, decoders, latches, D flip-flop, registers, shift registers.
Design with hardware description languages: (Verilog) module definitions, gate-level circuits, assign statements, behavioural combinational descriptions, behavioural synchronous descriptions.
Design flow and FPGA architecture: basic circuit synthesis, FPGA logic blocks, hard blocks, I/O,

mapping to FPGA blocks, placement and routing, configuring FPGAs.
Testing digital circuits: basic Verilog testbenches, self-checking testbenches, file I/O for input/output vectors, testing strategies.
Arithmetic circuits: limits of ripple adders, carry-lookahead adders, multipliers, fixed-point data representation and resulting errors, floating point circuit complexity.
Timing and pipelining: basic combinational timing characteristics, timing of synchronous components, computing circuit timing performance, pipelining for improved performance, hazards, race conditions, and metastability.
Processors and I/O: basic structure of a processor and how this relates to performance, integrating peripherals over UART, SPI, I2C, and faster serial standards, computing data rates for these standards.

Learning outcomes

By the end of the module, students should be able to:

- Understand the theory of combinational and sequential circuits and how these combine in the design of digital computing circuits through the use of the Verilog hardware description language (HDL).
- Assess the digital design flow as currently practised professionally in industry, with reference to field programmable gate arrays, and at a more general level, to custom application specific integrated circuits.
- Examine how mathematics is performed in custom circuits, and how simple units can be combined to implement compute datapaths.
- Develop a testing strategy and design a testbench to evaluate the functional correctness of a circuit using the testing features of the Verilog HDL and a professional standard simulator.
- Discuss the performance of synchronous digital circuits, based on the timing of basic components, and how pipelining affects performance, and how this differs from measuring the performance of software running on processors.

Subject specific skills

Plan and manage the design process, including cost drivers, evaluating outcomes, and working with technical uncertainty.
Ability to apply relevant practical and laboratory skills.
Ability to conceive, make and realise a component, product, system or process.

Transferable skills

Numeracy: apply mathematical and computational methods to communicate parameters, model and optimize solutions.
Apply problem-solving skills, information retrieval, and the effective use of general IT facilities.
Communicate (written and oral; to technical and non-technical audiences) and work with others.
Plan self-learning and improve performance, as the foundation for lifelong learning/CPD.
Exercise initiative and personal responsibility, including time management, which may be as a team member or leader.
Overcome difficulties by employing skills, knowledge and understanding in a flexible manner.

Study

Study time

Type	Required
Lectures	20 sessions of 1 hour (13%)
Practical classes	7 sessions of 2 hours (9%)
Other activity	2 hours (1%)
Private study	114 hours (76%)
Total	150 hours

Private study description

Guided independent learning: 114 hrs

Other activity description

Revision classes: 2 × 1 hr

Costs

No further costs have been identified for this module.

Assessment

You must pass all assessment components to pass the module.

Assessment group C3

	Weighting	Study time
Assessed Design Assignment (10 page report)	50%	

Assessed Design Assignment, to design and implement a digital circuit of moderate complexity using the skills learnt in the course.

Online Examination	50%	

QMP online examination

~Platforms - AEP,QMP

- Online examination: No Answerbook required

	Weighting	Study time

- Students may use a calculator
- Engineering Data Book 8th Edition

Feedback on assessment

Detailed marking on assessed design exercise.
Model solutions are published for past examination papers
Cohort level feedback on examinations

Past exam papers for ES2E3

Availability

Courses

This module is Core for:

- Year 2 of UCSA-G406 Undergraduate Computer Systems Engineering
- Year 2 of UCSA-G408 Undergraduate Computer Systems Engineering