

# ES434-15 ASICS, MEMS and Smart Devices

**22/23**

**Department**

School of Engineering

**Level**

Undergraduate Level 4

**Module leader**

Julian Gardner

**Credit value**

15

**Module duration**

10 weeks

**Assessment**

50% coursework, 50% exam

**Study location**

University of Warwick main campus, Coventry

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## Description

### Introductory description

n/a

[Module web page](#)

### Module aims

The course aims to present, mainly through sharing substantial practical experience, the design methodology of Application Specific Integrated Circuits (ASICs) and Micro-Electro-Mechanical Systems (MEMS).

### Outline syllabus

This is an indicative module outline only to give an indication of the sort of topics that may be covered. Actual sessions held may differ.

Devices and silicon processing; ASIC (based on analogue/digital VLSI) and MEMS design; silicon micromachining and other emerging process technologies; system design methodology; device design styles: detailed optimisation (cost and power), principles and applications. Examples

include both physical and chemical microsensors, MEMS and microsystems, in the application domains of consumer electronics, automotive, environmental, industrial, and healthcare. Students are expected to read chapters and solve problems taken from the recommended text-book. Written Design Project: ASIC chip, MEMS or smart device to be designed and simulated in laboratories with students working individually.

## **Learning outcomes**

By the end of the module, students should be able to:

- Critique the main principles of ASICs, smart systems and devices.
- Design ASICS and MEMS through practical experience using typical modern Computer Aided Design software for this task.
- Understand emerging techniques in ASICs, MEMS and smart sensor systems.
- Evaluate the principles and processes involved in the implementation of complex VLSI circuits and MEMS devices.

## **Indicative reading list**

A "Microsensors, MEMS and Smart Devices", Gardner, J.W. et al. 2001, 9780471861096, TK 7874.G2

B "CMOS Analog Circuit Design", Allen, P.E. , 2012, 978-0199765072,

B "CMOS VLSI design", Weste, N.H.E, 2011, 9780321547743, TK 7872.468.W3

B "Integrated Circuit Design", Weste, N.H.E, 2011, 978-0321696946,

C "MEMS Mechanical Sensors", Beeby, S, 2004, 9781580535366, TK 7874.M3

## **Subject specific skills**

1. Ability to conceive, design and model a Si CMOS or MEMS component, product, and process.
2. Ability to develop economically viable solutions to ASIC and MEMS components.
3. Ability to seek to achieve ASIC solutions to potential applications and have strategies for being creative and innovative.
4. Ability to be performance, cost and value design conscious, and aware of their environmental, health and safety, and wider professional engineering responsibilities.

## **Transferable skills**

1. Awareness of the nature of business and enterprise in the creation of economic and social value.
  2. Overcome difficulties by employing skills, knowledge and understanding in a flexible manner.
  3. Ability to formulate and operate within appropriate codes of conduct, when faced with an engineering issue.
  4. Appreciation of the international dimensions of engineering, commerce and communication.
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# Study

## Study time

| Type              | Required                    |
|-------------------|-----------------------------|
| Lectures          | 20 sessions of 1 hour (13%) |
| Seminars          | 10 sessions of 1 hour (7%)  |
| Practical classes | 5 sessions of 3 hours (10%) |
| Other activity    | 1 hour (1%)                 |
| Private study     | 104 hours (69%)             |
| Total             | 150 hours                   |

## Private study description

Self-study of 104 hours

## Other activity description

1x1 hour Revision Class

## Costs

No further costs have been identified for this module.

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## Assessment

You must pass all assessment components to pass the module.

Students can register for this module without taking any assessment.

## Assessment group C4

|   | Weighting | Study time |
|---|-----------|------------|
| Computer-based Design & Simulation Report   | 50%       |            |
| Will consist of the marks of the labs (attending the lab and working on lab exercises) and an up to 6 pages in length report                                    |           |            |
| In-person Examination   | 50%       |            |
| <ul style="list-style-type: none"><li>• Answerbook Green (8 page)</li><li>• Students may use a calculator</li><li>• Engineering Data Book 8th Edition</li></ul> |           |            |

## Feedback on assessment

Feedback during all laboratory sessions of progress.

Feedback from laboratory-based design report.

Cohort level feedback on laboratory reports and examinations.

[Past exam papers for ES434](#)

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## Availability

### Post-requisite modules

If you pass this module, you can take:

- ES3D8-15 Fundamentals of Modern VLSI Design

## Courses

This module is Core for:

- Year 4 of UESA-H63X MEng Electronic Engineering
- Year 5 of UESA-H636 MEng Electronic Engineering with Intercalated Year
- Year 5 of UESA-H63Y MEng Electronic Engineering with Intercalated Year
- Year 4 of UESA-H606 Undergraduate Electrical and Electronic Engineering MEng
- Year 5 of UESA-H607 Undergraduate Electrical and Electronic Engineering with Intercalated Year

This module is Optional for:

- Year 4 of UESA-H116 MEng Engineering with Exchange Year
- Year 5 of UESA-H115 MEng Engineering with Intercalated Year
- RESA-H6P9 Postgraduate Research Wide Bandgap Power Electronics
  - Year 1 of H6P9 Wide Bandgap Power Electronics (EngD)
  - Year 2 of H6P9 Wide Bandgap Power Electronics (EngD)
- Year 1 of TESA-H641 Postgraduate Taught Communications and Information Engineering
- Year 1 of TESA-H642 Postgraduate Taught Energy and Power Engineering

This module is Option list A for:

- Year 4 of UESA-H114 MEng Engineering
- Year 4 of UESA-H311 MEng Mechanical Engineering
- Year 4 of UCSA-G408 Undergraduate Computer Systems Engineering
- Year 5 of UCSA-G409 Undergraduate Computer Systems Engineering (with Intercalated Year)