ES3F1-15 High Performance Embedded Systems Design

22/23

Department
School of Engineering
Level
Undergraduate Level 3
Module leader
Eduardo Wachter
Credit value
15
Module duration
10 weeks
Assessment
50% coursework, 50% exam
Study location
University of Warwick main campus, Coventry

Description

Introductory description

EES3F1-15 High Performance Embedded Systems Design

Module web page

Module aims

To develop a student's ability in digital design to the level of designing high performance software/hardware embedded systems using hybrid FPGA reconfigurable devices combining processors and reconfigurable hardware fabric.

Outline syllabus

This is an indicative module outline only to give an indication of the sort of topics that may be covered. Actual sessions held may differ.

Design Flow and Verilog Recap: Revision of Register Transfer Level (RTL) design, behavioural modelling, hardware synthesis and implementation flow.
Design Space Exploration: Understanding area, performance, and power in the context of

embedded systems, and the trade-offs between them.
High Level Synthesis: C-to-gates and other languages, compiler outline, supported language features, basic scheduling.
Interconnect and Data Movement. Processor to logic interfacing, busses and crossbars, networks-on-chip, Direct Memory Access (DMA).
Modern Hybrid FPGA Architecture: Advanced DSP block architecture, advanced I/O, partial reconfiguration, hybrid FPGA architecture, PCIe-connected FPGAs.
Accelerating Algorithms: Standard DSP structures, including FIR filters, image filters, number representation and numerical precision.

Learning outcomes

By the end of the module, students should be able to:

- Apply the more advanced features of FPGA architectures in high performance embedded systems design.
- Design a hardware accelerator for an algorithm by evaluating its parallelism and arithmetic requirements, and measure its performance.
- Apply practical knowledge of hardware design at the register transfer level and using high level synthesis.
- Understand how to integrate a hardware accelerator with a processor and design the necessary software and hardware communication infrastructure.
- Understand the trade-offs between performance, area, and power in the design of hardware accelerators.

Indicative reading list

Embedded Systems Design with FPGAs, P Athanas, D. Pnevmatikatos, N. Sklavos (Editors), Springer, 2013.
Embedded Systems Fundamentals with Arm Cortex-M based Microcontrollers, A. G. Dean, Arm Education Media UK, 2017.
The Zynq Book: Embedded Processing with the ARM® Cortex-A9 on the Xilinx Zynq-7000 All Programmable SoC, Louise H. Crockett, Ross A. Elliot, Martin A. Enderwitz, Robert W. Stewart, Strathclyde Academic Media, 2014
Parallel Programming for FPGAs, R. Kastner, J. Matai, and S. Neuendorffer, arXiv, 2018.

Subject specific skills

Ability to conceive, make and realise a component, product, system or process
Ability to be pragmatic, taking a systematic approach and the logical and practical steps necessary for, often complex, concepts to become reality

Transferable skills

Communicate (written and oral; to technical and non-technical audiences) and work with others
Exercise initiative and personal responsibility, including time management, which may be as a team member or leader
Overcome difficulties by employing skills, knowledge and understanding in a flexible manner

Study

Study time

Type	Required
Lectures	10 sessions of 1 hour (7%)
Seminars	10 sessions of 1 hour (7%)
Practical classes	7 sessions of 2 hours (9%)
Other activity	2 hours (1%)
Private study	114 hours (76%)
Total	150 hours

Private study description

114 hours Guided Independent Learning

Other activity description

2 x 1 hour Revision classes

Costs

No further costs have been identified for this module.

Assessment

You must pass all assessment components to pass the module.

Assessment group C2

	Weighting	Study time
Design Assignment	50%	
Assessed design assignment to design and implement a digital circuit of advanced complexity using the skills learnt in the module (10 page design report)		
Online Examination	50%	
QMP online examination		
~Platforms - AEP,QMP		

	Weighting	Study time

- Online examination: No Answerbook required
- Students may use a calculator
- Engineering Data Book 8th Edition

Feedback on assessment

- Support through office hours.
- Detailed marking on assessed design assignment.
- Cohort-level feedback on final exam.

Past exam papers for ES3F1

Availability

Pre-requisites

To take this module, you must have passed:

- All of
  - ES2E3-15 Digital Systems Design

Courses

This module is Core for:

- Year 3 of UCSA-G406 Undergraduate Computer Systems Engineering
- Year 3 of UCSA-G408 Undergraduate Computer Systems Engineering
- Year 4 of UCSA-G407 Undergraduate Computer Systems Engineering (with Intercalated Year)
- Year 4 of UCSA-G409 Undergraduate Computer Systems Engineering (with Intercalated Year)