

ES3D8-15 Fundamentals of Modern VLSI Design

20/21

Department

School of Engineering

Level

Undergraduate Level 3

Module leader

Marina Cole

Credit value

15

Module duration

10 weeks

Assessment

100% coursework

Study location

University of Warwick main campus, Coventry

Description

Introductory description

n/a

[Module web page](#)

Module aims

The course aims to present the principles and techniques of integrated circuit (IC design), connecting digital system and logic design with the fundamental device physics, processing techniques and transistor level characteristics of Silicon integrated circuits, both in theoretical and practical aspects.

Outline syllabus

This is an indicative module outline only to give an indication of the sort of topics that may be covered. Actual sessions held may differ.

Silicon Processing. CMOS circuits for logic gates. Cell layout styles. Cell composition and

structured layout techniques. Transmission gate logic and dynamic memory. Latches. Complex CMOS gates. Dynamic logic. Timing analysis and optimisation. Logical Effort and Delay Estimation. Power dissipation. Sequential Logic Design. Subsystem design: adders, , RAM, datapath and PLA/ROM. Managing Complex Designs, Clocks, I/O, Packaging. Design Exercises to cover cell layout and composition, switch level simulation and timing analysis, critical path finding and circuit level simulation for timing and power.

Learning outcomes

By the end of the module, students should be able to:

- Examine how IC technology affects logic implementation and optimisation of simple CMOS integrated circuits.
- Apply simplified models to estimate the delay and power consumption of digital integrated circuits.
- Manage complex designs including partitioning into CMOS subsystems such as datapaths and memory arrays.
- Demonstrate basic knowledge how different circuit families can be used in IC design for trade-offs in speed, power, complexity and robustness.
- Acquire skills in the use of Computer Aided Design Software for IC design such as Mentor Graphics Tanner Tools or Cadence.
- Use CMOS technology, design and analysis techniques for implementation of digital IC systems.

Indicative reading list

"Fundamentals of Modern VLSI Devices, Taur, Y, 2013, 978-1107635715

"Integrated Circuit Design", Weste, N.H.E, 2011, 978-0321696946

"CMOS VLSI design", Weste, N.H.E, 2011, 9780321547743, TK 7872.468.W3

"CMOS: Circuit Design, Layout, and Simulation", Baker, R.J, 2011, 9781118038239

"Modern VLSI Design", Wolf,W, 2009, 978-0137145003,

Subject specific skills

Ability to conceive, make and realise a component, product, system or process

Ability to be pragmatic, taking a systematic approach and the logical and practical steps necessary for, often complex, concepts to become reality

Transferable skills

Numeracy: apply mathematical and computational methods to communicate parameters, model and optimize solutions

Apply problem solving skills, information retrieval, and the effective use of general IT facilities

Communicate (written and oral; to technical and non-technical audiences) and work with others

Plan self-learning and improve performance, as the foundation for lifelong learning/CPD

Exercise initiative and personal responsibility, including time management, which may be as a team member or leader

Overcome difficulties by employing skills, knowledge and understanding in a flexible manner

Study

Study time

Type	Required
Lectures	15 sessions of 1 hour (10%)
Practical classes	9 sessions of 3 hours (18%)
Private study	108 hours (72%)
Total	150 hours

Private study description

108 hours Guided Independent Learning

Costs

No further costs have been identified for this module.

Assessment

You must pass all assessment components to pass the module.

Assessment group A1

Assessment component	Weighting	Study time	Eligible for self-certification
Electronic Submission of Designs Part 1 (Schematic design and simulation results)	30%		No
Electronic Design - By successfully completing this assignment the student will demonstrate understanding of the role, and skills in the use of Electronic Design Automation (EDA) Software for Integrated Circuit Design. The student will also be able to appreciate the properties of CMOS technology and its effect on logic implementation, optimisation and system design.			

Weighting**Study time****Eligible for self-
certification**

Reassessment component is the same

Assessment component

Report related to Electronic Design 20%

No

Written Reflective Report 1500 words - Brief report reflecting on the design approach and on how could the designs be optimised further in terms of size, speed and power.

Reassessment component is the same

Assessment component

Electronic Submission of Designs

Part 2 (Layout design and post layout 30%
simulation results)

No

Electronic Design - By successfully completing this assignment the student will demonstrate understanding of the role, and skills in the use of Electronic Design Automation (EDA) Software for Integrated Circuit Design. The student will also be able to appreciate the properties of CMOS technology and its effect on logic implementation, optimisation and system design.

Reassessment component is the same

Assessment component

Test on basic knowledge of CMOS
technology 20%

No

The student will apply simplified models to estimate the delay and power consumption of digital integrated circuits. The student will also demonstrate basic knowledge how different circuit families can be used in IC design for trade-offs in speed, power, complexity and robustness.

Reassessment component is the same

Feedback on assessment

Feedback on assessment is by individual feedback mark sheet and overview. Feedback will be provided during the last 4 laboratory sessions and for the written report.

Availability

Courses

This module is Core for:

- Year 3 of UESA-H63W BEng Electronic Engineering
- Year 4 of UESA-H63V BEng Electronic Engineering with Intercalated Year
- Year 3 of UESA-H63X MEng Electronic Engineering
- UESA-H636 MEng Electronic Engineering with Intercalated Year
 - Year 3 of H636 Electronic Engineering with Intercalated Year
 - Year 4 of H636 Electronic Engineering with Intercalated Year

This module is Core optional for:

- UESA-H636 MEng Electronic Engineering with Intercalated Year
 - Year 3 of H636 Electronic Engineering with Intercalated Year
 - Year 4 of H636 Electronic Engineering with Intercalated Year
- Year 4 of UESA-H63Y MEng Electronic Engineering with Intercalated Year
- Year 3 of UESA-H115 MEng Engineering with Intercalated Year

This module is Optional for:

- Year 3 of UESA-H113 BEng Engineering
- Year 3 of UESA-H114 MEng Engineering
- Year 4 of UESA-H115 MEng Engineering with Intercalated Year

This module is Option list A for:

- Year 4 of UESA-H111 BEng Engineering with Intercalated Year
- Year 3 of UESA-H112 BSc Engineering
- Year 3 of UCSA-G406 Undergraduate Computer Systems Engineering
- Year 3 of UCSA-G408 Undergraduate Computer Systems Engineering
- Year 4 of UCSA-G407 Undergraduate Computer Systems Engineering (with Intercalated Year)
- Year 4 of UCSA-G409 Undergraduate Computer Systems Engineering (with Intercalated Year)